

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
13 December 2001 (13.12.2001)

PCT

(10) International Publication Number
WO 01/95398 A1

(51) International Patent Classification⁷: **H01L 29/78**, (21/336, 29/06, 21/225)

(81) Designated States (*national*): AE, AG, AI, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(21) International Application Number: **PCT/US01/17745**

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

(22) International Filing Date: 1 June 2001 (01.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/586,407 2 June 2000 (02.06.2000) US
09/849,036 4 May 2001 (04.05.2001) US

(71) Applicant: **GENERAL SEMICONDUCTOR, INC.**
[US/US]; 10 Melville Park Road, Melville, NY 11747
(US).

(72) Inventor: **BLANCHARD, Richard, A.**; 10724 Mora Drive, Los Altos, CA 94024 (US).

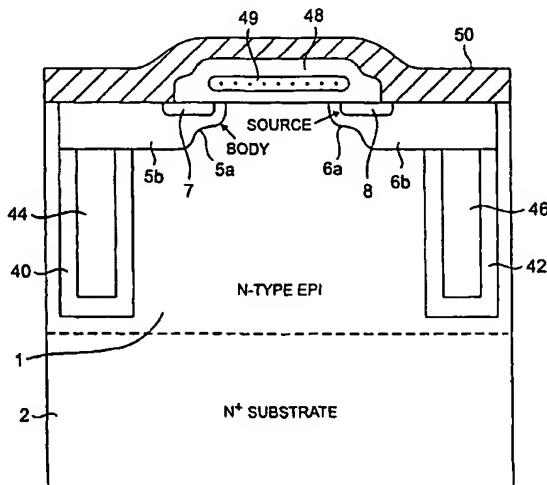
(74) Agent: **MAYER, Stuart, H.**; Mayer, Fortkort & Williams, PC, Suite 250, 200 Executive Drive, West Orange, NJ 07052 (US).

Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: POWER MOSFET AND METHOD OF MAKING THE SAME



WO 01/95398 A1

(57) Abstract: A power MOSFET is provided that includes a substrate (2) of a first conductivity type. An epitaxial layer (1) also of the first conductivity type is deposited on the substrate. First and second body regions (5a, 6a, 5b, 6b) are located in the epitaxial layer and define a drift region between them. The body regions have a second conductivity type. First and second source regions (7, 8) of the first conductivity type are respectively located in the first and second body regions. A plurality of trenches (44, 46) are located below the body regions in the drift region of the epitaxial layer. The trenches, which extend toward the substrate from the first and second body regions, are filled with an epitaxially layered material that includes a dopant of the second conductivity type. The dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches so as to form semiconductor regions (40, 42) of the second conductivity type under the body regions.

HIGH VOLTAGE POWER MOSFET HAVING LOW ON-RESISTANCE

Related Applications

[0001] This application is a continuation-in-part of U.S. Appl. Serial No.09/586,407 entitled "High Voltage Power MOSFET Having Low On-Resistance," filed on June 2, 2000.

Field of the Invention

[0002] The present invention relates generally to semiconductor devices, and more particularly to power MOSSFET devices.

Background of the Invention

[0003] Power MOSFET devices are employed in applications such as automobile electrical systems, power supplies, and power management applications. Such devices should sustain high voltage in the off-state and yield low voltage and high saturation current density in the on-state.

[0004] FIG. 1 illustrates a typical structure for an N-channel power MOSFET. An N-epitaxial silicon layer 1 formed over an N+ silicon substrate 2 contains p-body regions 5a and 6a, and N+ source regions 7 and 8 for two MOSFET cells in the device. P-body regions 5 and 6 may also include deep p-body regions 5b and 6b. A source-body electrode 12 extends across certain surface portions of epitaxial layer 1 to contact the source and body regions. The N-type drain for both cells is formed by the portion of N-epitaxial layer 1 extending to the upper semiconductor surface in FIG. 1. A drain electrode (not separately shown) is provided at the bottom of N+ substrate 2. An insulated gate electrode 18 comprising oxide and polysilicon layers lies over the channel and drain portions of the body.

[0005] The on-resistance of the conventional MOSFET shown in FIG. 1 is

determined largely by the drift zone resistance in epitaxial layer 1. The drift zone resistance is in turn determined by the doping and the layer thickness of epitaxial layer 1. However, to increase the breakdown voltage of the device, the doping concentration of epitaxial layer 1 must be reduced while the layer thickness is increased. Curve 20 in FIG. 2 shows the on-resistance per unit area as a function of the breakdown voltage for a conventional MOSFET. Unfortunately, as curve 20 shows, the on-resistance of the device increases rapidly as its breakdown voltage increases. This rapid increase in resistance presents a problem when the MOSFET is to be operated at higher voltages, particularly at voltages greater than a few hundred volts.

[0006] FIG. 3 shows a MOSFET that is designed to operate at higher voltages with a reduced on-resistance. This MOSFET is disclosed in paper No. 26.2 in the Proceedings of the IEDM, 1998, p. 683. This MOSFET is similar to the conventional MOSFET shown in FIG. 2 except that it includes p-type doped regions 40 and 42 which extend from beneath the body regions 5 and 6 into to the drift region of the device. The p-type doped regions 40 and 42 define columns in the drift region that are separated by n-type doped columns such as column, which are defined by the portions of the epitaxial layer 1 adjacent the p-doped regions 40 and 42. The alternating columns of opposite doping type cause the reverse voltage to be built up not only in the vertical direction, as in a conventional MOSFET, but in the horizontal direction as well. As a result, this device can achieve the same reverse voltage as in the conventional device with a reduced layer thickness of epitaxial layer 1 and with increased doping concentration in the drift zone. Curve 25 in FIG. 2 shows the on-resistance per unit area as a function of the breakdown voltage of the MOSFET shown in FIG. 3. Clearly, at higher operating voltages, the on-resistance of this device is substantially reduced relative to the device shown in FIG. 1, essentially increasing linearly with the breakdown voltage.

[0007] The improved operating characteristics of the device shown in FIG. 3 are based on charge compensation in the drift region of the transistor. That is, the doping in the drift region is substantially increased, e.g., by an order of magnitude or more, and the additional charge is counterbalanced by the addition of columns of

opposite doping type. The blocking voltage of the transistor thus remains unaltered. The charge compensating columns do not contribute to the current conduction when the device is in its on state. These desirable properties of the transistor depend critically on the degree of charge compensation that is achieved between adjacent columns of opposite doping type. Unfortunately, nonuniformities in the dopant gradient of the columns can be difficult to avoid as a result of limitations in the control of process parameters during their fabrication. For example, diffusion across the interface between the columns and the substrate and the interface between the columns and the p-body region will give rise to changes in the dopant concentration of the portions of the columns near those interfaces.

[0008] The structure shown in FIG. 3 can be fabricated with a process sequence that includes multiple epitaxial deposition steps, each followed by the introduction of the appropriate dopant. Unfortunately, epitaxial deposition steps are expensive to perform and thus this structure is expensive to manufacture.

[0009] Accordingly, it would be desirable to provide a method of fabricating the MOSFET structure shown in FIG. 3 that requires a minimum number of deposition steps so that it can be produced less expensively while also allowing sufficient control of process parameters so that a high degree of charge compensation can be achieved in adjacent columns of opposite doping type in the drift region of the device.

Summary of the Invention

[0010] In accordance with the present invention, a power MOSFET is provided that includes a substrate of a first conductivity type. An epitaxial layer also of the first conductivity type is deposited on the substrate. First and second body regions are located in the epitaxial layer and define a drift region between them. The body regions have a second conductivity type. First and second source regions of the first conductivity type are respectively located in the first and second body regions. A plurality of trenches are located below the body regions in the drift region of the epitaxial layer. The trenches, which extend toward the substrate from the first and second body regions, are filled with an epitaxially layered material that includes a

dopant of the second conductivity type. The dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches, thus forming the p-type doped regions that cause the reverse voltage to be built up in the horizontal direction as well as the vertical direction.

[0011] In accordance with one aspect of the invention, the material filling the trench is silicon.

[0012] In accordance with yet another aspect of the invention, the silicon filling the trench is at least partially oxidized.

[0013] In accordance with another aspect of the invention, the material filling the trench is a dielectric such as silicon dioxide, for example.

[0014] In accordance with another aspect of the invention, the material filling the trench may include both silicon and a dielectric.

[0015] In accordance with another aspect of the invention, a method is provided for forming a power MOSFET. The method begins by providing a substrate of a first conductivity type and depositing an epitaxial layer on the substrate. The epitaxial layer has a first conductivity type. First and second body regions are formed in the epitaxial layer to define a drift region therebetween. The body regions have a second conductivity type. First and second source regions of the first conductivity type are formed in the first and second body regions, respectively. A plurality of trenches are formed in the drift region of the epitaxial layer. A material having a dopant of the second conductivity type is epitaxially deposited in the trenches. The trenches extend toward the substrate from the first and second body regions. At least a portion of the dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches.

Brief Description of the Drawings

[0016] FIG. 1 shows a cross-sectional view of a conventional power MOSFET structure.

[0017] FIG. 2 shows the on-resistance per unit area as a function of the breakdown voltage for a conventional power MOSFET and a MOSFET constructed in accordance with the present invention.

[0018] FIG. 3 shows a MOSFET structure designed to operate with a lower on-resistance per unit area at the same voltage than the structure depicted in FIG. 1.

[0019] FIGs. 4-6 show the pertinent portions of various embodiments of the power MOSFET constructed in accordance with the present invention.

[0020] FIG. 7 shows a complete power MOSFET constructed in accordance with the present invention.

Detailed Description

[0021] In accordance with the present invention, the p-type regions 40 and 42 shown in FIG. 3 are formed by first etching a pair of trenches that are centered about the position where the p-type regions 40 and 42 are to be located. The trenches are subsequently filled with a dopant rich material. The dopant in the material is diffused out of the trenches and into the adjacent epitaxial layer that forms the drift region of the device. The resulting doped portions of the epitaxial layer form the p-type regions. The material filling the trenches, along with the dopant that has not been diffused out of the trenches, remain in final device.

Accordingly, the material should be selected so that it does not adversely affect the characteristics of the device. Exemplary materials that may be used for the material filling the trenches include polysilicon or a dielectric such as silicon dioxide.

[0022] FIGs. 4-6 show several different combinations of materials that may be used to fill trenches 44 and 46 that are formed in epitaxial silicon layer 1. While FIGs. 4-6 show the trenches 44 and 46, epitaxial layer 1, and substrate 2, for purposes of clarity FIGs. 4-6 do not show the upper portion of the power MOSFET structure that includes the P-body regions and the sources.

[0023] In the embodiment of the invention shown in FIG. 4, the trenches 44 and 46 are filled with a doped dielectric such as boron-doped silicon dioxide. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The boron-doped silicon dioxide that fills the trench remains in the final MOSFET device.

[0024] In the embodiment of the invention shown in FIG. 5, the trenches are at

least partially filled with polycrystalline silicon, i.e., polysilicon, that is doped with boron. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The remaining boron-doped polysilicon that fills the trench remains in the final MOSFET device. Alternatively, the polysilicon may be all or partially oxidized after the diffusion step is performed to form silicon dioxide. Accordingly, the trench remaining in the final MOSFET device is filled with a dielectric, i.e., silicon dioxide, and any residual polysilicon. In another alternative, any boron-doped polysilicon in the trench is recrystallized at an elevated temperature to form single crystal silicon. In this case the trench remaining in the final MOSFET device is filled with single crystal silicon, or single crystal silicon in combination with silicon dioxide or another dielectric.

[0025] In the embodiment of the invention shown in FIG. 6, the trenches 44 and 46 are first partially filled with doped polysilicon followed by the deposition of a dielectric to completely fill the trench. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The remaining boron-doped polysilicon and the dielectric filling the trench remains in the final MOSFET device. In some cases the boron-doped polysilicon is recrystallized at an elevated temperature to form single crystal silicon. Accordingly, the trench remaining in the final MOSFET device is filled with both single crystal silicon and a dielectric.

[0026] FIG. 7 shows the resulting power MOSFET constructed in accordance with the present invention. The MOSFET includes substrate 2, epitaxial layer 1, p-body regions 5a and 6a, deep p-body regions 5b and 6b, source regions 7 and 8, and p-type regions 40 and 42 in which trenches 44 and 46 are respectively located. P-type regions 40 and 42 define columns that are each separated by n-type doped columns. Also shown are the gate electrode, which includes oxide layer 48 and polysilicon layer 49, and the source-body electrode, which includes metallization layer 50.

[0027] In yet another embodiment of the invention, the trenches 44 and 46 may be filled with an epitaxially deposited material such as doped silicon. Epitaxial deposition may be advantageously employed in some cases because it both reduces

defect formation and enhances the control of the dopant gradient in the trenches so that better uniformity can be achieved. As previously mentioned, control over the dopant gradient is important because the reduced on-resistance of the device at higher operating voltages depends critically on the degree of charge compensation that is achieved between adjacent columns of opposite doping type. Accordingly, while this embodiment of the invention does require the utilization of an additional epitaxial deposition step, it can advantageously allow better charge compensation to be achieved.

[0028] The additional control offered by filling the trench with an epitaxially deposited material can be used to compensate for dopant non-uniformities that can arise in the portions of the columns near the interfaces with the substrate and the p-body region. Such non-uniformities can be caused by the diffusion that inevitably arises between the different layers when dopant is diffused out of the trenches to form the columns. For example, in FIG. 7 when dopant is diffused from the trenches 44 and 46 to form the p-type regions 40 and 42, additional dopant from the heavily-doped p-body regions 5 and 6 also diffuses into p-type regions 40 and 42. Accordingly, the portions of p-type regions 40 and 42 near the p-body regions 5 and 6 will be more heavily doped than the remainder of p-type regions 40 and 42.

[0029] The aforementioned problem may be overcome by epitaxially depositing a material into the trench with a gradually decreasing dopant concentration. This can be accomplished using a "graded epi" technique. That is, during the epitaxial deposition, the dopant concentration can be gradually increased or decreased. In this way a single dopant source with a specified concentration of atoms can be used to produce a range of dopant levels. Alternatively, this could be accomplished by arranging two or more sources with silicon that are doped to different concentrations. During the latter stages of the epitaxial deposition process the source or sources with a lower dopant concentration could be primarily used to reduce the dopant concentration of the resulting layer in the trench near the p-body regions. When the subsequent diffusion step is performed to define the columns, additional dopant material from the p-body regions will diffuse into the p-type columns, compensating for the inherently lower dopant concentration in the

epitaxially deposited layer. Of course, those of ordinary skill in the art will recognize that to obtain columns that are uniformly doped various process parameters such as the number of different sources, their dopant concentrations and the duration of the deposition steps from the different sources need to be optimized.

[0030] This same technique may be employed to compensate for the decreased dopant concentration that would otherwise arise in the portions of the p-type columns near the substrate. In this case, at the beginning of the epitaxial deposition process to fill the trenches, the source or sources with a higher dopant concentration could be primarily used to increase the dopant concentration of the resulting epitaxial layer located in the trench near the substrate.

[0031] The inventive power MOSFET shown in FIG. 7 may be fabricated in accordance with any conventional processing technique. For example, the following series of exemplary steps may be performed to form the power MOSFET depicted in FIG. 7.

[0032] First, an oxide masking layer is formed by covering the surface of epitaxial layer 1 with an oxide layer, which is then conventionally exposed and patterned to leave mask portions that define the location of the trenches 44 and 46. The trenches are dry etched through the mask openings by reactive ion etching to a depth that typically ranges from 10-40 microns. The sidewalls of each trench may be smoothed. First, a dry chemical etch may be used to remove a thin layer of oxide (typically about 500 – 1000 Å) from the trench sidewalls to eliminate damage caused by the reactive ion etching process. Next, a sacrificial silicon dioxide layer is grown over trenches 44 and 46 and the mask portions. The sacrificial layer and the mask portions are removed either by a buffer oxide etch or an HF etch so that the resulting trench sidewalls are as smooth as possible.

[0033] The trenches 44 and 46 are filled with any of the previously mentioned materials such as polysilicon, silicon dioxide, silicon, or a combination thereof. During deposition, the polysilicon or oxide are typically doped with a dopant such as boron. A subsequent diffusion step is performed to diffuse the dopant out the trenches and into the surrounding epitaxial layer. If the material remaining in the trenches is polysilicon, it may be oxidized or recrystallized.

[0034] Next, a photoresist masking process is used to form a patterned masking layer that defines source regions 7 and 8. Source regions 7 and 8 are then formed by an implantation and diffusion process. For example, the source regions may be implanted with arsenic at 80 KeV to a concentration that is typically in the range of 2×10^{15} to $1.2 \times 10^{16}/\text{cm}^2$. After implantation, the arsenic is diffused to a depth of approximately 0.5 to 2.0 microns. The depth of the deep p-body region typically ranges from about 2.5 to 5 microns while the depth of the body region ranges from about 1-3 microns in depth. Finally, the masking layer is removed in a conventional manner to form the structure depicted in FIG. 7.

[0035] The DMOS transistor is completed in a conventional manner by forming and patterning the oxide layer to form contact openings. A metallization layer 50 is also deposited and masked to define the source-body and gate electrodes. Also, a pad mask is used to define pad contacts. Finally, a drain contact layer (not shown) is formed on the bottom surface of the substrate.

[0036] It should be noted that while in the previously described process the trenches are formed prior to the formation of the p-body and deep p-body regions, the present invention more generally encompasses processes in which the trenches are formed prior to, or subsequent to, any or all of the remaining doped regions. In addition, while a specific process sequence for fabricating the power MOSFET is disclosed, other process sequences may be used while remaining within the scope of this invention.

[0037] The power MOSFET device constructed in accordance with the present invention offers a number of advantages over the prior art device constructed by conventional techniques. For example, the vertical dopant gradient of the p-type regions is very nearly zero. The horizontal dopant gradient may be accurately controlled by varying the amount of dopant that is introduced and the number and duration of thermal cycles used in the diffusion step. Furthermore, the amount of dopant introduced and the lateral dopant gradient can be varied to optimize both the breakdown voltage and the on-resistance of the device.

[0038] In the embodiment of the invention shown in FIG. 7 the p-type trench is

formed below the body region. However, not every p-type trench need have a body region associated with it, particularly at the perimeter of the die or in regions containing pads or interconnections.

[0039] Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention. For example, a power MOSFET in accordance with the present invention may be provided in which the conductivities of the various semiconductor regions are reversed from those described herein.

WHAT IS CLAIMED IS:

1. A power MOSFET, comprising:
 - a substrate of a first conductivity type;
 - an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;
 - first and second body regions located in the epitaxial layer defining a drift region therebetween, said body regions having a second conductivity type;
 - first and second source regions of the first conductivity type respectively located in the first and second body regions; and
 - a plurality of trenches located below said body regions in said drift region of the epitaxial layer, said trenches being filled with an epitaxially layered material having a dopant of the second conductivity type, said trenches extending toward the substrate from the first and second body regions, said dopant being diffused from said trenches into portions of the epitaxial layer adjacent the trenches.
2. The power MOSFET of claim 1 wherein said material filling the trench is silicon.
3. The power MOSFET of claim 1 wherein said material filling the trench is a dielectric.
4. The power MOSFET of claim 3 wherein said dielectric is silicon dioxide.
5. The power MOSFET of claim 1 wherein said dopant is boron.
6. The power MOSFET of claim 2 wherein said silicon is at least partially oxidized.
7. The power MOSFET of claim 1 wherein said material filling the trench includes silicon and a dielectric.

8. The power MOSFET of claim 1 wherein said body regions include deep body regions.
9. The power MOSFET of claim 1 wherein said epitaxially layered material includes a plurality of layers, at least two of said layers having different dopant concentrations.
10. The power MOSFET of claim 9 wherein said plurality of layers includes an interface layer adjacent to one of the body regions, said interface layer having a lower dopant concentration than an interior layer of the epitaxially layered material.
11. The power MOSFET of claim 1 wherein said epitaxially layered material has a dopant concentration that is reduced in the vicinity of the body regions relative to the dopant concentration profile in the vicinity of the substrate.
12. The power MOSFET of claim 1 wherein said portions of the epitaxial layer adjacent the trenches have a substantially uniform dopant concentration in a direction lateral to the trenches.
13. The power MOSFET of claim 11 wherein said portions of the epitaxial layer adjacent the trenches have a substantially uniform dopant concentration in a direction lateral to the trenches.
14. A method of forming a power MOSFET comprising the steps of:
 - providing a substrate of a first conductivity type;
 - depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;
 - forming first and second body regions in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type;
 - forming first and second source regions of the first conductivity type in the

first and second body regions, respectively; and
forming a plurality of trenches in said drift region of the epitaxial layer;
epitaxially depositing in said trenches a material having a dopant of the
second conductivity type, said trenches extending toward the substrate from the first
and second body regions; and
diffusing at least a portion of said dopant from said trenches into portions of
the epitaxial layer adjacent the trenches.

15. The method of claim 14 wherein said epitaxially deposited material filling
the trench includes silicon.

16. The method of claim 14 wherein said material filling the trench is a
dielectric.

17. The method of claim 16 wherein said dielectric is silicon dioxide.

18. The method of claim 14 wherein said dopant is boron.

19. The method of claim 15 further comprising the step of at least partially
oxidizing said silicon

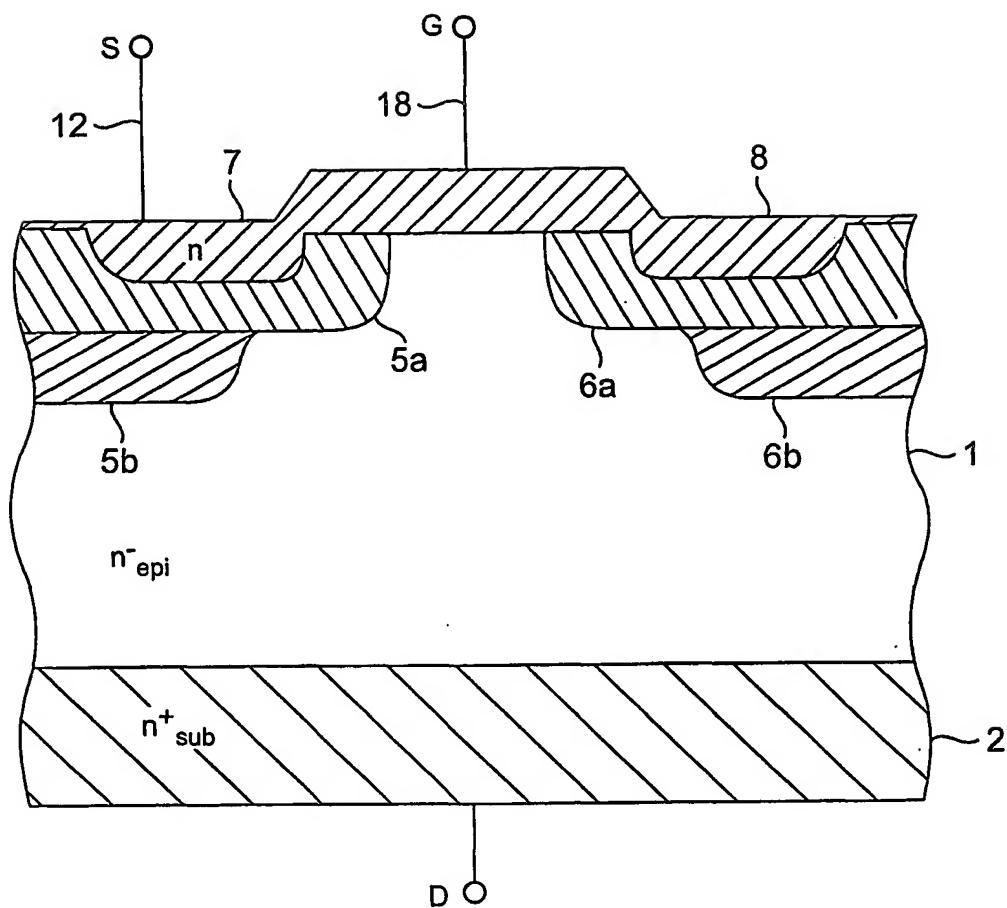
20. The method of claim 14 wherein said material filling the trench includes
silicon and a dielectric.

21. The method of claim 14 wherein said body regions include deep body
regions.

22. The method of claim 14, wherein said trench is formed by providing a
masking layer defining at least one trench, and etching the trench defined by the
masking layer.

23. The method of claim 14, wherein said body region is formed by implanting and diffusing a dopant into the substrate.
24. The method of claim 14 wherein the epitaxially depositing step includes the step of epitaxially depositing a plurality of layers, at least two of said layers having different dopant concentrations.
25. The method of claim 24 wherein said plurality of layers includes an interface layer adjacent to one of the body regions, said interface layer having a lower dopant concentration than an interior layer of the epitaxially layered material.
26. The method of claim 14 wherein said epitaxially layered material has a dopant concentration that is reduced in the vicinity of the body regions relative to the dopant concentration profile in the vicinity of the substrate.
27. The method of claim 1 wherein said portions of the epitaxial layer adjacent the trenches have a substantially uniform dopant concentration in a direction lateral to the trenches.
28. The method of claim 26 wherein said portions of the epitaxial layer adjacent the trenches have a substantially uniform dopant concentration in a direction lateral to the trenches.
29. A power MOSFET made in accordance with the method of claim 14.

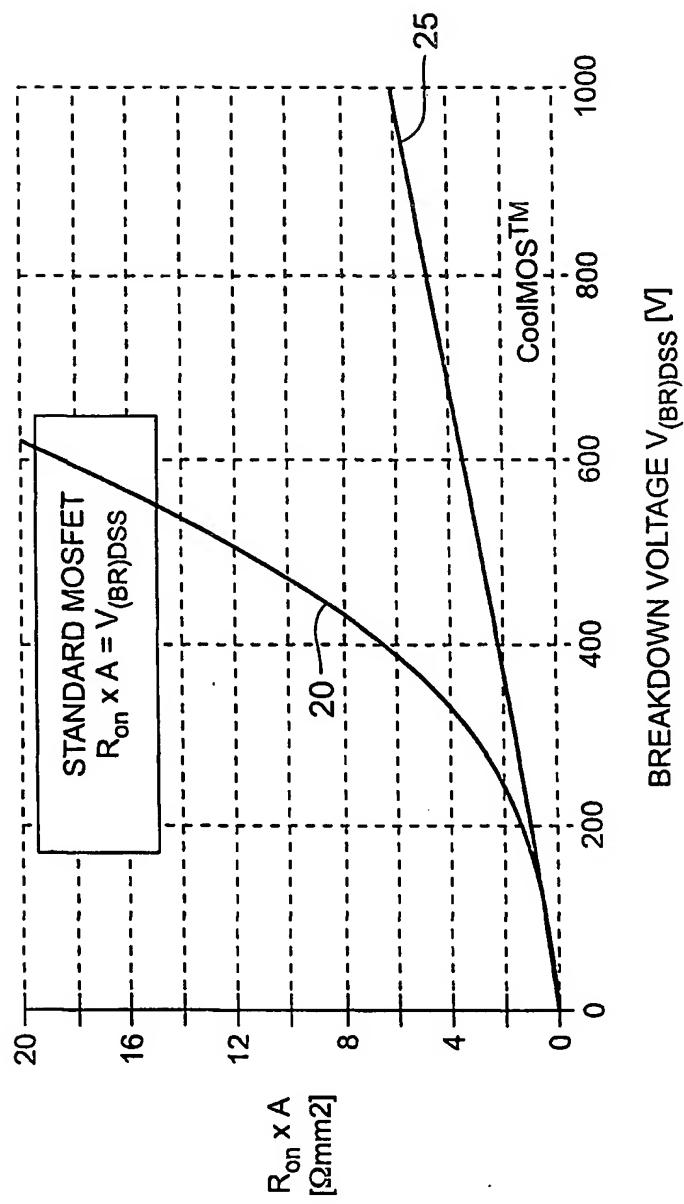
1/7



CONVENTIONAL MOSFET

FIG. 1

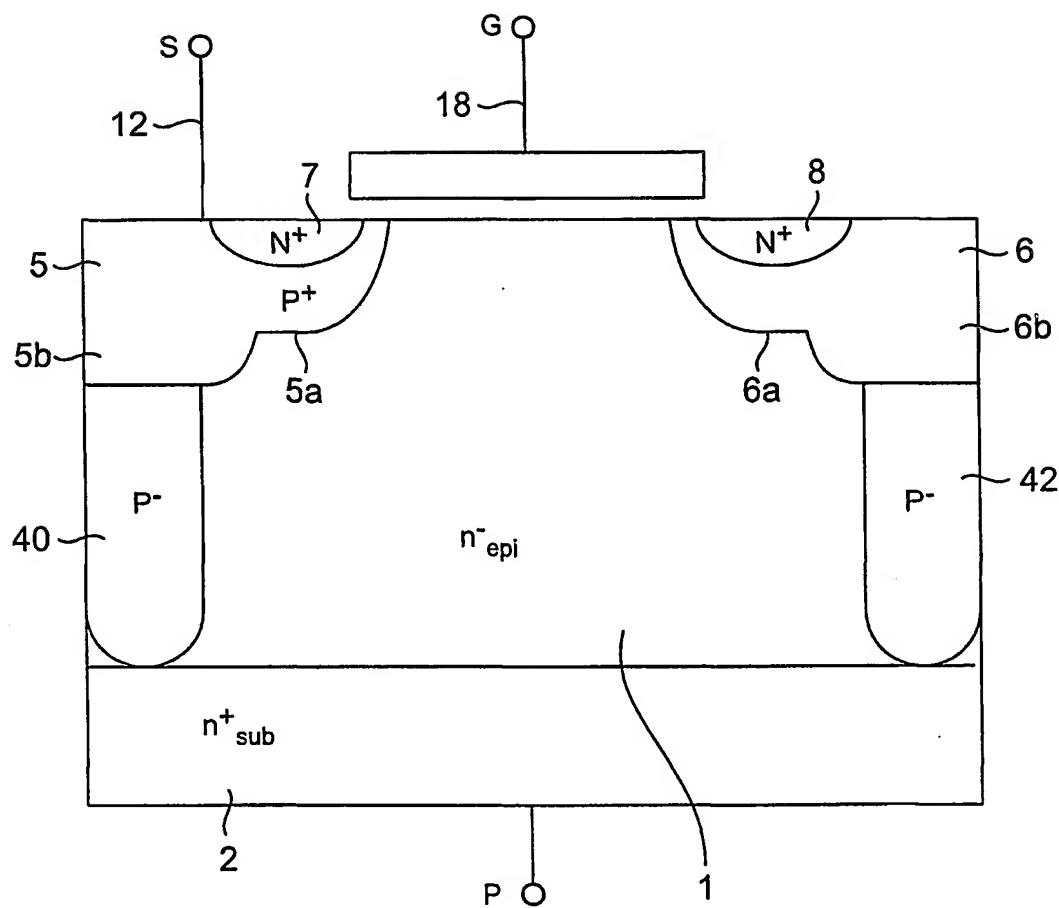
2/7



THE SPECIFIC ON-RESISTANCE OF A VERTICAL DMOS TRANSISTOR WITH THE DOPANT DISTRIBUTION OF FIG. 1

FIG. 2

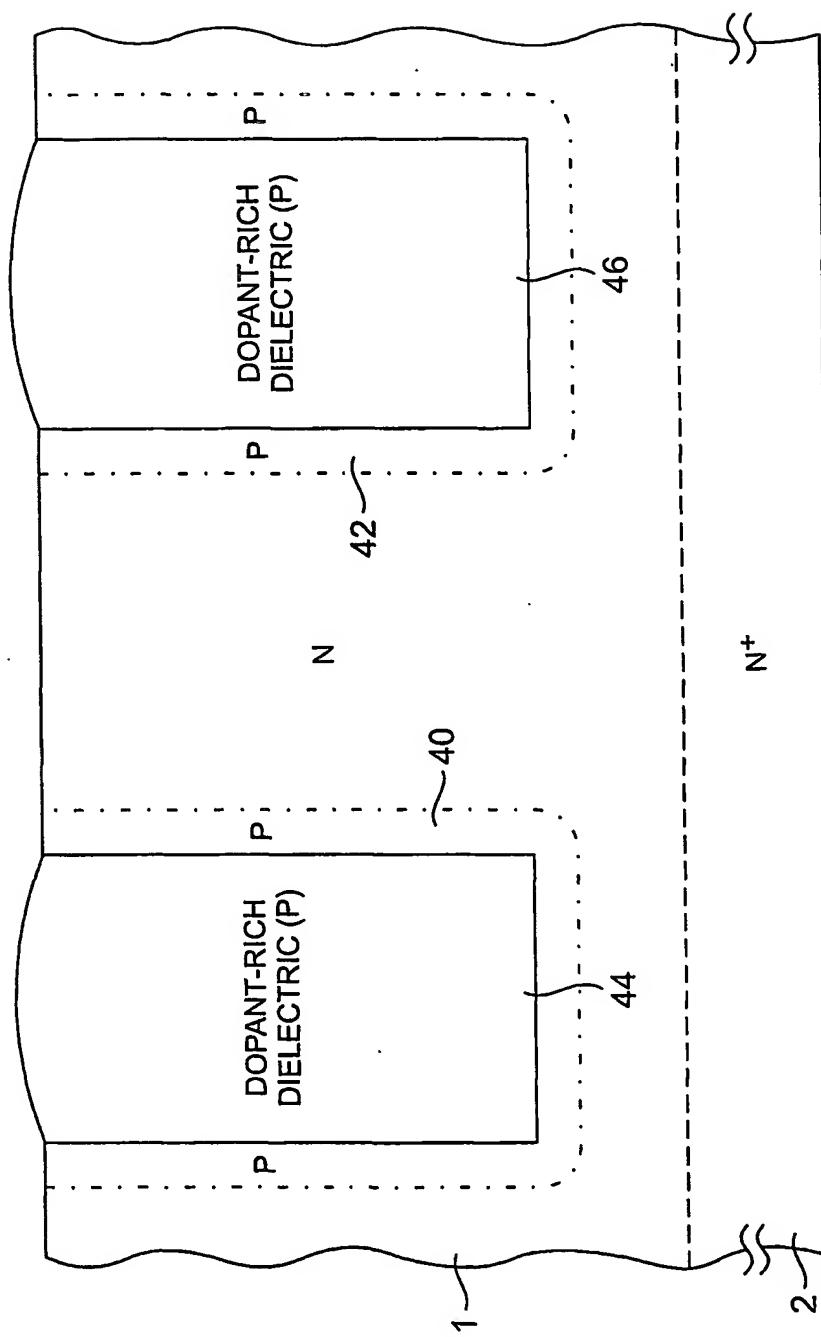
3/7



THE DOPANT DISTRIBUTION OF A
HIGH VOLTAGE VERTICAL DMOS TRANSISTOR
WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 3

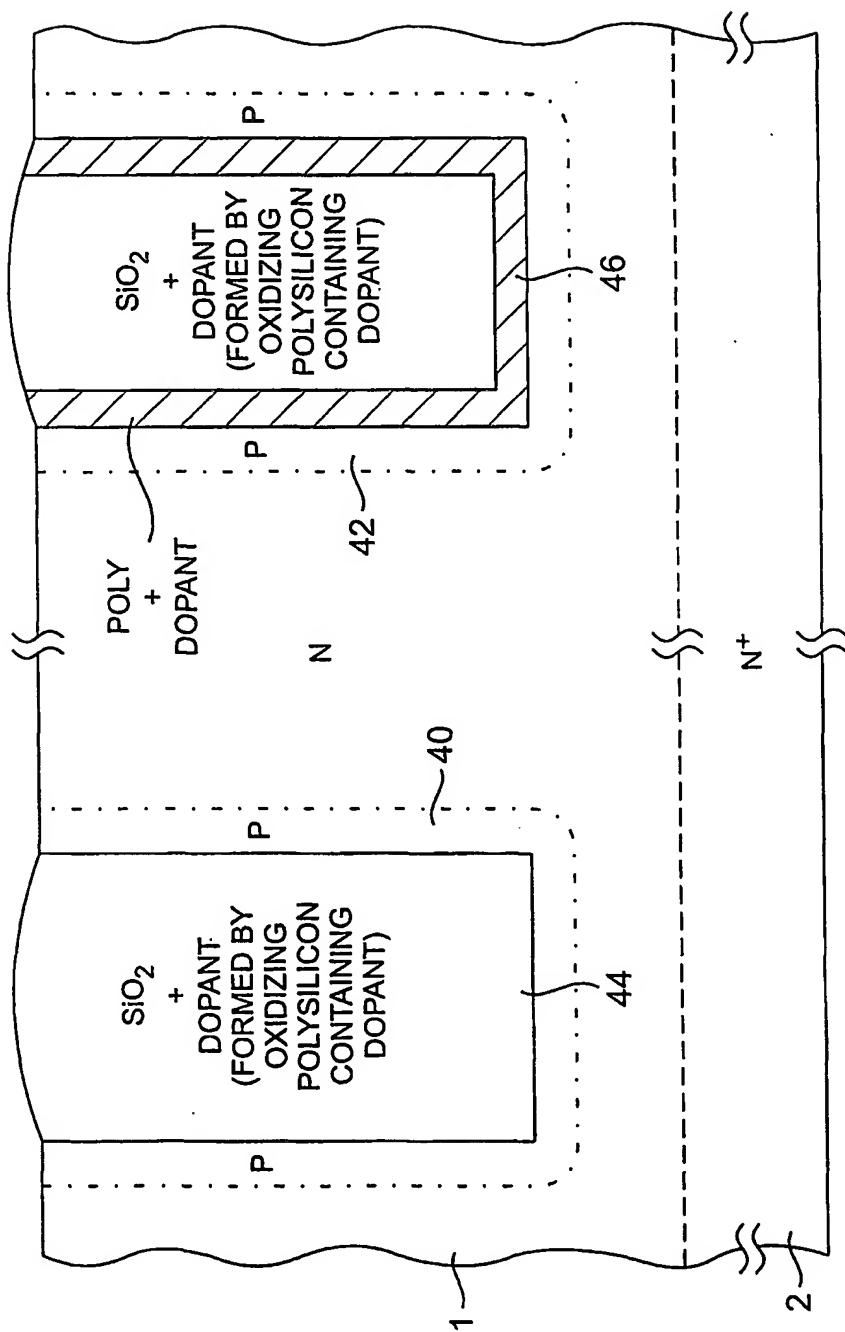
4/7



A DOPING PROFILE THAT WAS DIFFUSED FROM
TRENCHES FILLED WITH DOPANT-RICH DIELECTRIC

FIG. 4

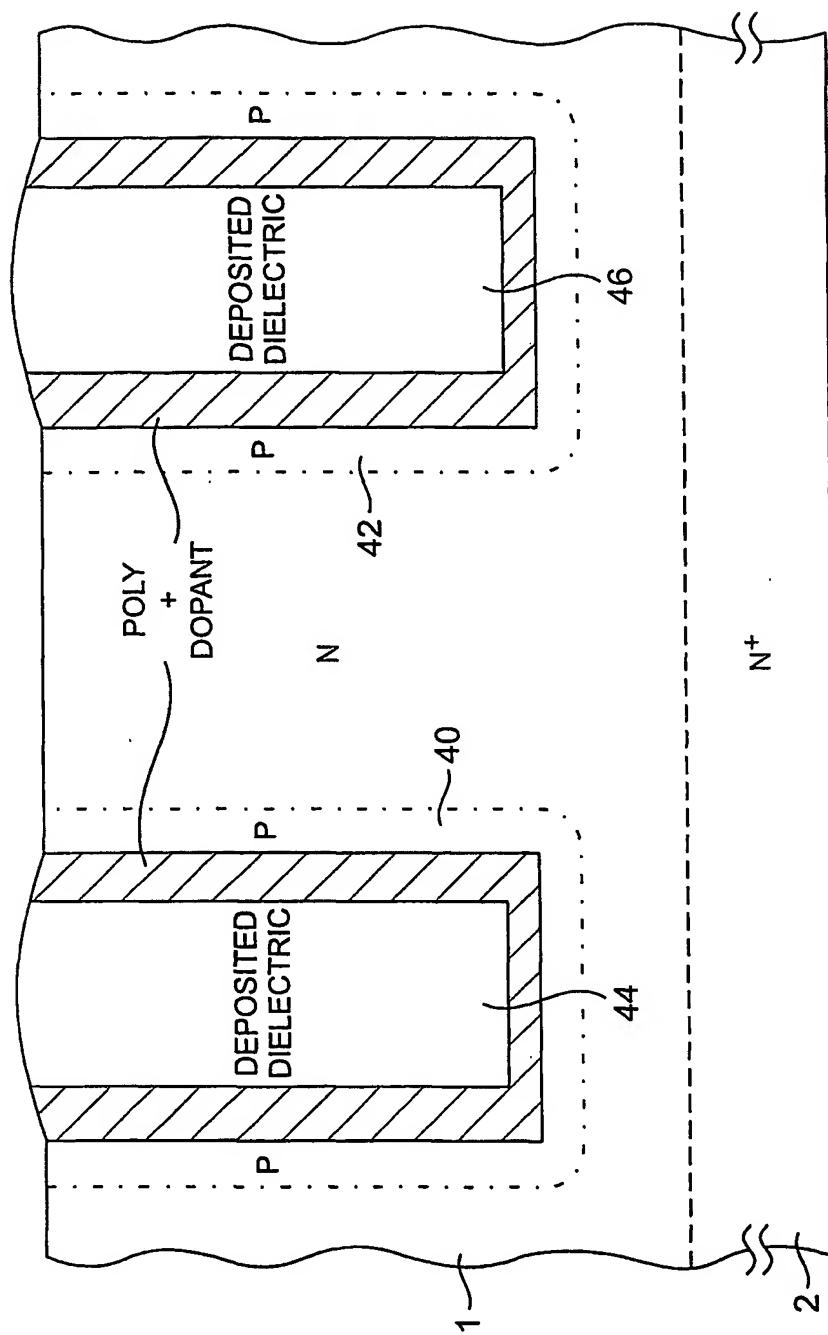
5/7



A DOPING PROFILE THAT WAS DIFFUSED FROM TRENCHES CONTAINING DOPED POLYCRYSTALLINE SILICON THAT WAS SUBSEQUENTLY OXIDIZED

FIG. 5

6/7



A DOPING PROFILE THAT WAS DIFFUSED FROM A
TRENCH CONTAINING DOPED POLYCRYSTALLINE
SILICON AS WELL AS DEPOSITED DIELECTRIC

FIG. 6

7/7

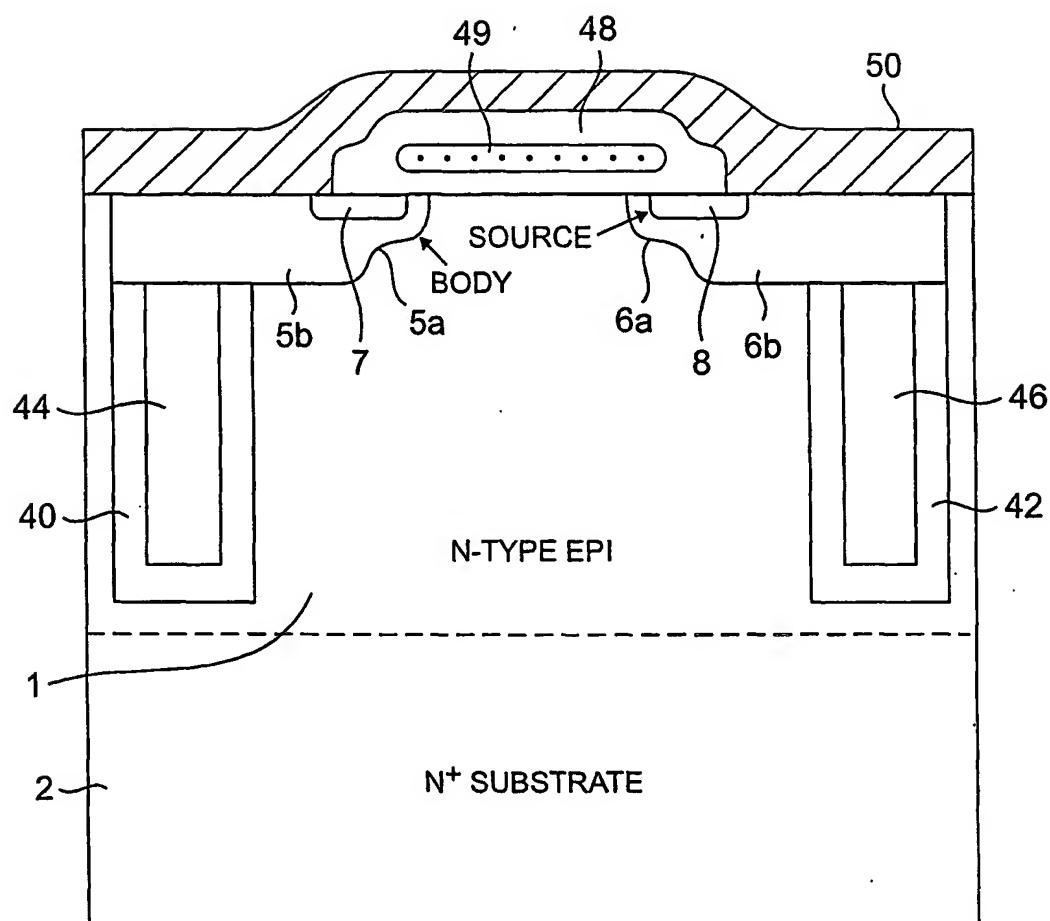


FIG. 7

INTERNATIONAL SEARCH REPORT

Int'l Application No
PCT/US 01/17745

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L21/336 H01L29/06 H01L21/225

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>US 5 216 275 A (CHEN X) 1 June 1993 (1993-06-01)</p> <p>column 5, line 30 -column 6, line 2; figures 2-5 column 3, line 38 - line 47 ---</p> <p style="text-align: center;">-/-</p>	<p>1,2,5-9, 12,14, 15, 18-24, 27,29</p>

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the International filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the International filing date but later than the priority date claimed

- *T* later document published after the International filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *&* document member of the same patent family

Date of the actual completion of the International search	Date of mailing of the International search report
18 October 2001	26/10/2001
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Morvan, D

INTERNATIONAL SEARCH REPORT

Inten Application No
PCT/US 01/17745

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GLENN J ET AL: "A novel vertical deep trench RESURF DMOS (VTR-DMOS)" PROCEEDINGS OF THE 12TH INTERNATIONAL SYMPOSIUM ON POWER SEMICONDUCTOR DEVICES & ICS, TOULOUSE, FR, 22 - 25 May 2000, pages 197-200, XP000974099 IEEE, Piscataway, NJ, USA ISBN: 0-7803-6269-1 paragraph II; figure 1 -----	14,15, 18-23, 27,29
A		1,2,5-8, 12

INTERNATIONAL SEARCH REPORTInt'l Application No
PCT/US 01/17745

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5216275	A 01-06-1993 CN	1056018 A	06-11-1991